tion. Excess currents near the pinch-off region are attributed to an energy level located around 0.25 eV below the conduction band, whose origin is not known.

ACKNOWLEDGMENT

Contributions are acknowledged from J. F. Ryan in epitaxial growth of silicon on sapphire, from H. G. Dill in the mask design and assistance in the fabrication of the MOS structures. Preliminary mobility data were furnished by P. Knoll and the electrical measurements were carried out by F. A. Rhoads.

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Extended Coverage Corner Reflector

Conventional corner reflectors are retrodirective for all angles of incidence less than or equal to 45° with respect to the optical axis of the corner. Radiation incident at larger angles is scattered in all directions.

It is the purpose of this communication to note that the solid angle over which a corner reflector is retrodirective can be increased by filling the corner with a dielectric material having a flat front face. Refraction at this flat face reduces the apparent angle of incidence of any radiation on the corner and extends the corners coverage angle.

The principle of operation is illustrated in Fig. 1. Radiation striking the front face of the dielectric material with an angle of incidence i strikes the corner reflector at an apparent angle of incidence r, where

$$\sin r = \sin i/\sqrt{\epsilon} \qquad (1)$$

where ϵ is the dielectric constant of the material employed. Thus, an $\epsilon=2$, reduces an $i=90°$ to an r of 45°, which lies within the coverage angle of a conventional corner. Thus, the corner reflector will reply retrodirectively and a second refraction at the dielectric face will send the radiation back to its source. At this extreme angle, the dielectric filled corner acts like a retrodirective end fire array.

Experimental confirmation of this theory was obtained with a dihedral corner filled with a material with an $\epsilon=1.9$. The corner had sides 6 inches wide and 7 inches high,

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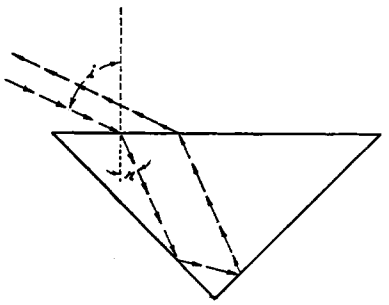

Fig. 1. Radiation path in dielectric filled corner reflector.

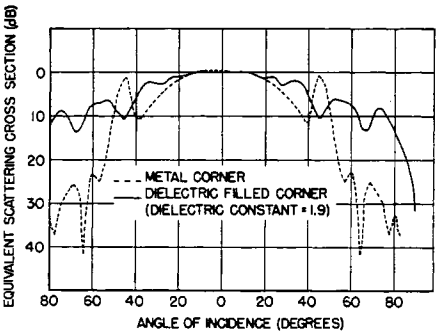

Fig. 2. Experimental results.

and the measurements were made at 10 Gc. Figure 2 is a plot of the results obtained with and without the dielectric in the corner. The increased coverage provided by the dielectric is dramatically evident and substantiates the theory.

Control of ϵ now allows control of coverage angle and permits a designer to use the smallest number of corners to cover a given solid angle with a minimum amount of scintillation. For example, 3 corners could be used to cover 4π steradians by choosing ϵ so that each corner covers $4\pi/3$ steradians. With normal corners, this coverage would require 8 corners and 2.66 times the volume.

This volume is critical in many instances such as targets, aircraft, satellites, etc., and this saving would be valuable. In addition, the use of artificial dielectrics will insure low weight per corner.

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Measurements of Propagation Delay Time in Transistors

The measurement of signal propagation times in transistors is often complicated by signal delays in the circuit path. Circuit paths consisting of passive elements and stray parameters are lumped transmission lines which may have relatively slow propagation rates. The delay times created by

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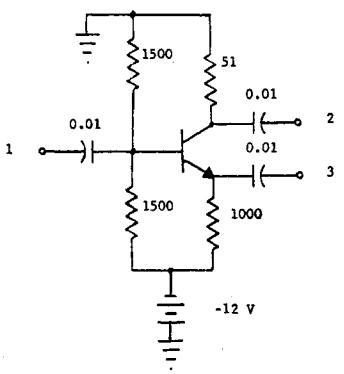


Fig. 1. Test circuit.

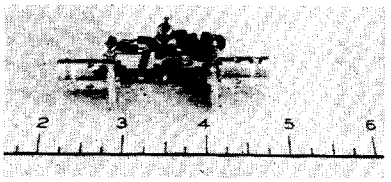


Fig. 2. Test circuit layout.

these lumped transmission lines are usually not negligible when considering transistor propagation delay times of less than 1 ns.

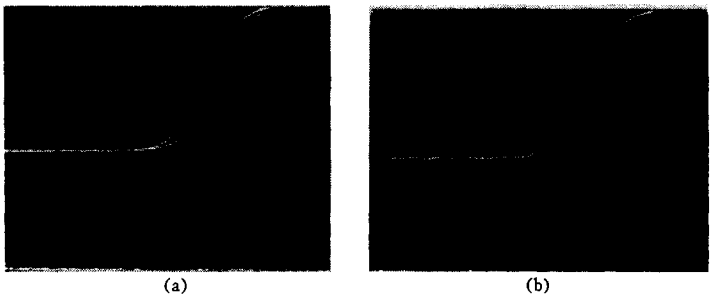
The circuit of Fig. 1 was used to measure the propagation delay times of transistors in the common base (CB) and the common collector (CC) configurations. The circuit was compactly constructed between two BNC connectors as shown in Fig. 2. For the CC configuration, terminal 2 of Fig. 1 was grounded; terminal 1 was used as the input; and terminal 3 was used as the output. For the CB configuration, terminal 1 was grounded; terminal 3 served as the input; and terminal 2 served as the output. Each input and output terminal was loaded with 50 ohms.

The circuit was pulsed with a Hewlett-Packard model 215A pulse generator, and the resulting waveforms were observed with a Tektronix 661 sampling oscilloscope. With the oscilloscope externally triggered, a reference waveform was established by short-circuiting together the input and output terminals of the transistor at the transistor socket. This reference waveform was positioned with the 10 per cent point of the leading edge at the center of the scope screen. Then, with the short circuit removed from the transistor socket, the gain of the oscilloscope preamplifier was adjusted to normalize the transistor output trace to the same level as established by the reference waveform. Thus, a time displacement due only to the transistor was observed at the 10 per cent point on the leading edge of the output pulse.

Three commonly used high-speed transistors were tested in both the CB and CC configurations. The results are shown in Figs. 3 through 5. The trace passing through the center point of the oscilloscope screen in these figures represents the reference trace mentioned previously. The time measured along the central horizontal axis to the second trace represents propagation delay time of the transistor at the 10 per cent point of the rising wavefront. An output of 200 mV was used in all cases. For each transistor tested, the input signal was chosen to pro-

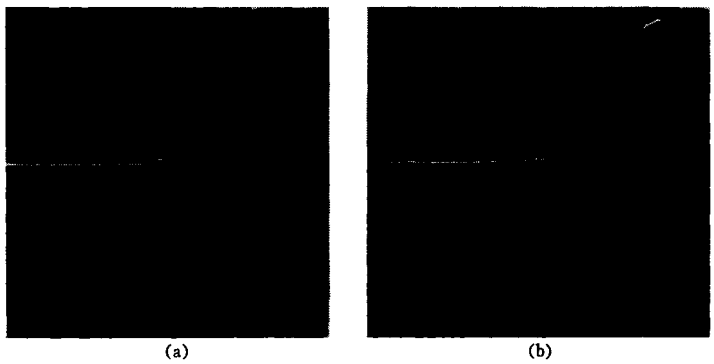
(a) (b)

Fig. 3. Propagation delay time measurements of a 2N976 transistor operated in (a) CC mode, and (b) CB mode. Time scale: 0.5 ns/cm.



(a) (b)

Fig. 4. Propagation delay time measurements of a 2N709 transistor operated in (a) CC mode, and (b) CB mode. Time scale: 0.5 ns/cm.



(a) (b)

Fig. 5. Propagation delay time measurements of a 2N2857 transistor operated in (a) CC mode, and (b) CB mode. Time scale: 0.5 ns/cm.

duce a greater emitter current.

As might be expected, a longer time delay was observed for the CB configuration than for the CC configuration. This added delay (also the slower rise time) is conceivably due to charge diffusion across the base region.

The delay time of the circuit layout was also measured. With a short-circuiting wire placed across the transistor socket, a reference trace was obtained on the oscilloscope. The input and output cables were then disconnected and joined together directly. The resulting trace indicated a time displacement of approximately 0.4 ns, which is greater than any of the delay times measured for the transistors tested. Consequently, had the circuit path been considered as representing negligible time delay, the transistor propagation delay time measured would have been seriously in error.

A collector current and collector voltage of 5 mA and 6 volts, respectively, was used in obtaining the waveforms of Figs. 3 through 5. A variation in these values of approximately 50 percent did not appreciably affect the observed signal delay time at the 10 per cent point on the leading edge of the pulse. This fact is illustrated in Fig. 6, which represents the signal delay in a 2N2857 transistor operated in the CB mode. The reference trace is shown passing through the center of the screen, as before. The delayed trace taken from the transistor output, however, actually consists of three lines corresponding to supply voltages (Fig. 1) of 6, 12, and 18 volts.

Fig. 6. Propagation delay time measurement of a 2N2857 transistor with various bias conditions. Time scale: 0.5 ns/cm.

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The Charge-Storage Diode as a Subharmonic Generator

The use of the charge-storage diode as a highly efficient harmonic generator has been reported by several authors [1]–[4]. Its application in subharmonic generation is less well known.

While the proper characterization of the charge-storage (step-recovery, snap-off) diode is not clearly established, any nonlinear capacitance property would make subharmonic generation possible [5], [6] and the Manley-Rowe [7] relations would apply. Moreover, its efficiency as a harmonic generator should result in locking of the low-frequency output to the pump frequency with much lower pump levels than required by varactors.

This communication describes experimental work demonstrating subharmonic generation with charge-storage diodes. Experimental circuits have been fabricated and operated successfully for various division ratios. A particularly impressive example is a divide-by-13 circuit operating with 6 per cent efficiency. In this case a 2280 Mc/s input signal at 35 mW produced a locked output of 2.1 mW at 175.4 Mc/s.

The circuit arrangement employed uses a single reactively tuned idler at $(n-1)\omega$ where ω is the output frequency and $n\omega$ is the input frequency. This corresponds to the inverting demodulator case of Manley & Rowe. Essentially equivalent results were obtained using both the hpa 0153 step-recovery diode and the GE SSA 550 snap-off diode.

While a rigorous theoretical treatment is lacking at present, experience with the tune-up of this subharmonic generator indicates that its behavior is consistent with the Manley-Rowe theory for this class of device. As optimum tuning is approached, tunable oscillations occur which give way to an oscillation whose frequency is not affected by tuning. Maximum efficiency is obtained on the verge of instability.

Since the charge-storage diode generates harmonics readily, the output of the subharmonic generator can be expected to contain a number of harmonics of the desired output frequency, unless adequate precautions are taken. With the divide-by-13 circuit described above, a high-quality coaxial low-pass filter was used to ensure elimination of unwanted harmonics.

It should be noted that the 6 per cent efficiency mentioned above approaches $1/n$, a value frequently quoted as a typical efficiency for the charge-storage diode as a high-order multiplier.

Further clues as to the mechanism involved were sought by the use of a divide-by-five circuit operating with 575 Mc/s input, an idler at 460 Mc/s and output at 115 Mc/s. In this case provision was made for resistive termination of the idler frequency. With this arrangement, an output of 6 mW was obtained at 115 Mc/s with 36 mW input at 575 Mc/s. Again, this efficiency of 16.7 per cent approaches $1/n$.

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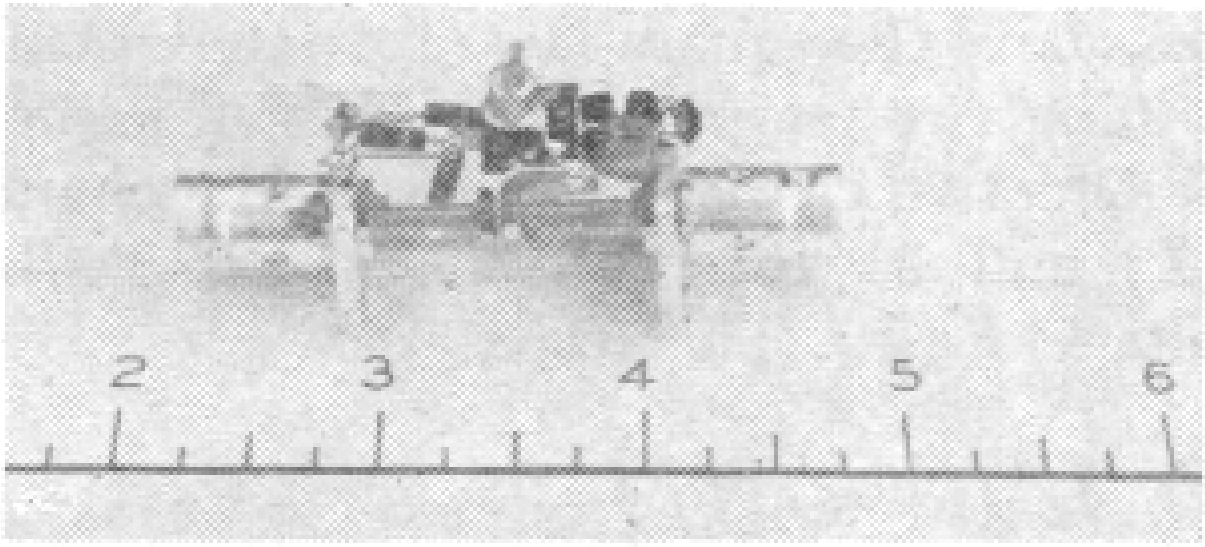
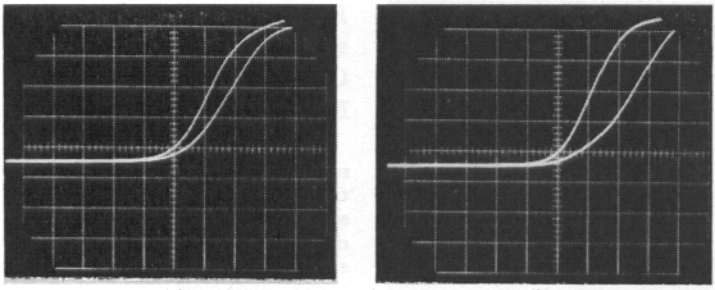
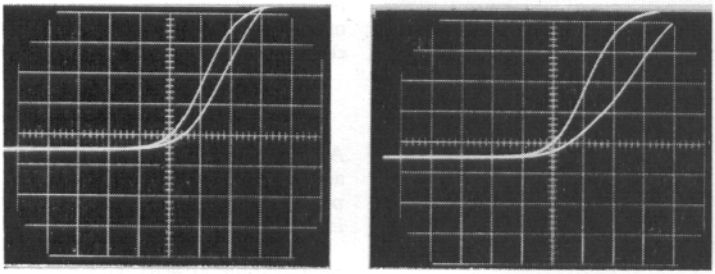


Fig. 2. Test circuit layout.



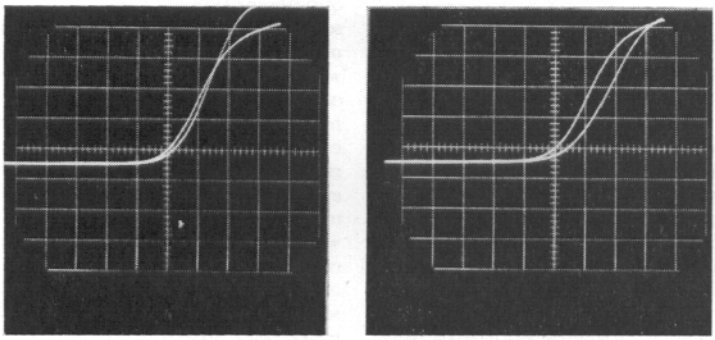
(a) (b)

Fig. 3. Propagation delay time measurements of a 2N976 transistor operated in (a) CC mode, and (b) CB mode. Time scale: 0.5 ns/cm.



(a) (b)

Fig. 4. Propagation delay time measurements of a 2N709 transistor operated in (a) CC mode, and (b) CB mode. Time scale: 0.5 ns/cm.



(a) (b)

Fig. 5. Propagation delay time measurements of a 2N2857 transistor operated in (a) CC mode, and (b) CB mode. Time scale: 0.5 ns/cm.

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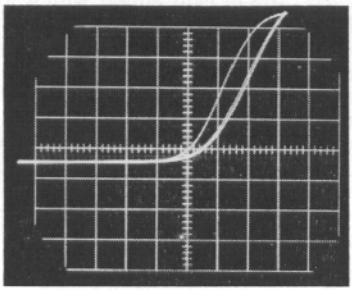

Fig. 6. Propagation delay time measurement of a 2N2857 transistor with various bias conditions. Time scale: 0.5 ns/cm.